UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,636	03/17/2004	Chang-Lien Wu	REAP0049USA	2635

27765 7590 12/19/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,636	WU ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 13-26 are presented for examination. This office action is in response to the RCE filed on 11/17/2006.

2. The status of the referenced U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any.

Information Disclosure Statement

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 13-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (Kim) US Patent No. 6,781,898 or rejected under 35 U.S.C. 102(a) as being anticipated by Chin US Patent Pub. No. 2003/0145250.

As to claim 13, Kim discloses a method for generating a linked list (col. 2 lines 8+ and Fig. 2 Ref. 170) corresponding to a memory in an electronic device (col. 1 line 23), comprises forming a linked list (Fig. 1b) for the memory, wherein each entry of the linked list corresponds to a portion of the memory (Fig. 1b); performing a built-in self test (BIST) (Fig. 2 Refs 172 and 182) on the memory to identify a first defective portion of the memory (Fig. 1b); and updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory (Fig. 3 and col. 6 lines 36-44) before the memory is completely examined by the BIST (Fig. 1b col. 5 lines 24-38).

Alternatively, Chin discloses a method for generating a linked list (Fig. 3) corresponding to a memory in an electronic device (block 4), comprises forming a linked list for the memory (fig. 3 and block 11), wherein each entry of the linked list corresponds to a portion of the memory; performing a built-in self test (BIST) (block 11) on the memory to identify a first defective portion of the memory; and updating the linked list (block 12-15 and Fig. 4) to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory before the memory is completely examined by the BIST(Fig. 5 loop between Refs. 21 and 24 and Fig. 5 loop between Refs. 32 and 34).

As to claim 14, Kim discloses the invention as claimed above. Kim further discloses wherein the memory being tested in the above step is used for storing the linked list (Fig. 2 Refs. 150 & 166 and Fig. 3 Ref. 222), and the above step comprises excluding the use of the deflective portion of the memory in storing the linked list (Fig. 1b, skip).

As to claim 15, Kim discloses the invention as claimed above. Kim further discloses wherein the memory being tested in the above step is a packet buffer for data storage (Fig. 2 Ref. 180)

As to claim 16, Kim discloses the invention as claimed above. Kim further discloses wherein the above step of updating is performed before the BIST performed in the above is completely through with the entirety of the memory (Fig. 3 Refs. 223 and 245 and col. 6 lines 36-45).

As to claim 17, Kim discloses the invention as claimed above. Kim further discloses after performing the step of updating, continuing the BIST in the step to identify a second defective portion of the memory (Fig. 3 Ref. 223); and updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified second defective portion of the memory (Fig. 3 ref. 203)

As to claim 18, Kim discloses the invention as claimed above. Kim further discloses wherein the electronic device comprising the memory is a network switch (col. 1 lines 11 and 23-24).

As to claim 19, Kim discloses a method for generating a linked list (col. 2 lines 8+ and Fig. 2 Ref. 170) corresponding to a memory in an electronic device (col. 1 line 23), comprises forming a linked list (Fig. 1b) for the memory, wherein the linked list comprises a plurality of entries (Fig. 1b) each having a first pointer field and a second pointer field (Fig. 1b) , the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list; performing a built-in self test (BIST) (Fig. 2 Refs 172 and 182)on the memory to identify at least one defective portion of the memory; and updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified defective portion of the memory, so that none of the entries of the updated linked list comprises a pointer in the second pointer field that points to the entry corresponding to the identified defective portion (Fig. 3 and col. 6 lines 36-44) wherein the step of updating the linked list is performed before the memory is completely examined by the BIST (Fig. 1b col. 5 lines 24-38)

As to claim 20, Kim discloses the invention as claimed above. Kim further discloses wherein the electronic device comprising the memory is a network switch (col. 1 lines 11 and 23-24).

As to claim 21, Kim discloses the invention as claimed above. Kim further discloses wherein the memory being tested in the BIST step is a packet buffer for data storage (Fig. 2 Ref. 180) .

As to claim 22, Kim discloses a method for generating a linked list (col. 2 lines 8+ and Fig. 2 Ref. 170) corresponding to a memory (col. 1 line 23), comprises forming a linked list (Fig. 1b) for the memory, wherein the linked list comprises a plurality of entries each having a first pointer field and a second pointer field (Fig. 1b), the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list; performing a built-in self test (BIST) (Fig. 2 Refs 172 and 182) on the memory to identify a first defective portion of the memory; updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory (Fig. 1b col. 5 lines 24-38 and col. 6 lines 36-44); after the above step is completed, continuing the BIST to identify a second defective portion of the memory (Fig. 3 refs. 223 and 245); and updating the linked list to remove front the linked list the entry of the linked list corresponding to the identified second defective portion of the memory (Fig. 3 and col. 6 lines 36-44).

As to claim 23, Kim discloses the invention as claimed above. Kim further discloses wherein the memory is a packet buffer for data storage (Fig. 2 Ref. 180).

As to claim 24, Kim discloses the invention as claimed above. Kim further discloses wherein step (b) comprises pausing the BIST when the first defective portion of the memory is identified (Fig. 1b, col. 5 lines 24-38 and col. 6 lines 36-44).

As to claim 25, Kim discloses a method for generating a linked list (col. 2 lines 8+ and Fig. 2 Ref. 170) corresponding to a memory(Fig. 1b Ref. 103), comprises forming a linked list (Fig. 1b) for the memory, wherein the linked list comprises a plurality of entries each having a first pointer field and a second pointer field (Fig. 1b) , the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list (Fig. 1b); performing a built-in self test (BIST) (Fig. 2 Refs. 172 and 182) on the memory; and each time a defective portion is found in the memory by the BIST pausing the BIST, updating the linked list to remove an entry corresponding to the defective portion of the memory from the linked list, and then continuing the BIST on remaining portions of the memory (Fig. 1b col. 5 lines 24-38).

Alternatively, Chin discloses a method for generating a linked list (Fig. 3) corresponding to a memory (Fig. 3 Ref. 1), comprises forming a linked list (Fig. 3 and block 11) for the memory, wherein the linked list comprises a plurality of entries each having a first pointer field and a second pointer field (Fig. 3) , the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list (Fig. 3); performing a built-in self test (BIST)

(block 11) on the memory; and each time a defective portion is found in the memory by the BIST pausing the BIST, updating the linked list to remove an entry corresponding to the defective portion of the memory from the linked list, and then continuing the BIST on remaining portions of the memory (Fig. 5 loop between Refs. 21 and 24 and Fig. 5 loop between Refs. 32 and 34).

As to claim 26, Kim discloses the invention as claimed above. Kim further discloses wherein the memory is a packet buffer for data storage (Fig. 2 Ref. 180).

Response to Arguments

5. Applicant's arguments filed on 11/17/06 have been fully considered but they are not persuasive.

Applicant's remarks on page 13 that the references not teaching updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory before the memory is completely examined by the BIST is not considered persuasive.

Kim discloses updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory (Fig. 3 and col. 6 lines 36-44) before the memory is completely examined by the BIST (Fig. 1b col. 5 lines 24-38 In other words, the linked listed is updated as each defective memory location is identified).

Alternatively, Chin discloses updating the linked list (block 12-15 and Fig. 4) to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory before the memory is completely examined by the BIST(Fig. 5 loop between Refs. 21 and 24, and Fig. 5 loop between Refs. 32 and 34). Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
December 13, 2006